
1. Overview

1.1 Features

The R8C/3MQ Group single-chip MCU functions as a low-power-consumption transceiver which supports 2.4 GHz compliant to IEEE802.15.4 standard and incorporates the R8C CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

The R8C/3MQ Group has data flash (1 KB × 4 blocks) with the background operation (BGO) function.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outline the Specifications for R8C/3MQ Group.

Table 1.1 Specifications for R8C/3MQ Group (1)

Item	Function	Specification
CPU	Central processing unit	R8C CPU core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 62.5 ns (f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) 125 ns (f(BCLK) = 8 MHz, VCC = 2.2 to 3.6 V) 250 ns (f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) • Multiplier: 16 bits × 16 bits → 32 bits • Multiply-accumulate instruction: 16 bits × 16 bits + 32 bits → 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte)
Memory	ROM, RAM, Data flash	Refer to Table 1.3 Product List for R8C/3MQ Group .
Power Supply Voltage Detection	Voltage detection circuit	<ul style="list-style-type: none"> • Power-on reset • Voltage detection 2 (detection level of voltage detection 1 selectable)
I/O Ports	Programmable I/O ports	CMOS I/O ports: 18 (including XCIN and XCOUT), selectable pull-up resistor (for some ports)
Clock	Clock generation circuits	<ul style="list-style-type: none"> • 3 circuits: XIN clock oscillation circuit, XCIN clock oscillation circuit (32 kHz), Low-speed on-chip oscillator • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, low-speed on-chip oscillator), wait mode, stop mode
		Real-time clock (timer RE)
Interrupts		<ul style="list-style-type: none"> • Interrupt Vectors: 69 • External: 11 sources (INT × 3, key input × 8) • Priority levels: 7 levels
Watchdog Timer		<ul style="list-style-type: none"> • 14 bits × 1 (with prescaler) • Reset start selectable • Low-speed on-chip oscillator for watchdog timer selectable
DTC (Data Transfer Controller)		<ul style="list-style-type: none"> • 1 channel • Activation sources: 17 • Transfer modes: 2 (normal mode, repeat mode)
Timer	Timer RA	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits × 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits × 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RE	8 bits × 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode

Table 1.2 Specifications for R8C/3MQ Group (2)

Item	Function	Specification
Serial Interface (UART0)		Shared with clock synchronous serial I/O mode and clock asynchronous serial I/O
Synchronous Serial Communication Unit (SSU)		1 (shared with I ² C bus)
I ² C bus		1 (shared with SSU)
RF	RF frequency	2405 MHz to 2480 MHz
	Reception sensitivity	-95 dBm
	Transmission output level	0 dBm
Baseband		<ul style="list-style-type: none"> • 127-byte transmit RAM, 127-byte receive RAM × 2 • Automatic ACK response function • 26-bit timer: Compare function in 3 channels
Encryption	AES	AES Encryption/Decryption (Key length 128bits)
Flash Memory		<ul style="list-style-type: none"> • Programming and erasure voltage: VCC = 1.8 to 3.6 V (in CPU rewrite mode) • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function
Operating Frequency/ Supply Voltage (in single mode)		f(BCLK) = 16 MHz, VCC = 2.7 to 3.6 V) f(BCLK) = 8 MHz (VCC = 2.2 to 3.6V) f(BCLK) = 4 MHz, VCC = 1.8 to 3.6 V) Note: f(XIN) = fixed at 16 MHz

Table 1.2 Specifications for R8C/3MQ Group (2)

Item	Function	Specification
Current Consumption (1)		RF = Tx: 18 mA RF = Rx (reception in progress): 25 mA RF = Rx (reception standby): 24 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 4 mA RF = off: 2.5 mA *The above applies when: f(XIN) = 16 MHz, f(BCLK) = 4 MHz, and VCC = VCCRF = 1.8 to 3.6 V
		RF = Tx: 19 mA RF = Rx (reception in progress): 26 mA RF = Rx (reception standby): 25 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 5 mA RF = off: 3.5 mA *The above applies when: f(XIN) = 16 MHz, f(BLCK) = 8 MHz, and VCC = VCCRF = 2.2 to 3.6 V
		RF = Tx: 21.5 mA RF = Rx (reception in progress): 28.5 mA RF = Rx (reception standby): 27.5 mA RF = Rx (reception standby)/wait mode: 23 mA RF = idle: 7.5 mA RF = off: 6 mA *The above applies when: f(XIN) = 16 MHz, f(BLCK) = 16 MHz, and VCC = VCCRF = 2.7 to 3.6 V
		Low-speed on-chip oscillator mode (f(BCLK) = 15.6 kHz): 80 μ A Low-speed clock mode (f(BCLK) = 32 kHz, flash memory low-power-consumption mode): 95 μ A Low-speed clock mode (f(BCLK) = 32 kHz, flash memory off/program operation on RAM): 45 μ A Wait mode (system clock = XCIN (32 kHz)), peripheral function clock on: 6 μ A Wait mode (system clock = XCIN (32 kHz)), peripheral function clock off: 4.5 μ A Wait mode (system clock = fOCO-S (125 kHz)), peripheral function clock on: 13 μ A Wait mode (system clock = fOCO-S (125 kHz)), peripheral function clock off: 7.5 μ A Stop mode (all clocks off): 2 μ A *When VCC = VCCRF = 1.8 to 3.6 V and RF = off
Operating Ambient Temperature		-20°C to 85°C (N version)
Package		40-pin HWQFN Package code: PWQN0040KB-A (previous code: 40PJS-A)

Note:

1. Refer to **5. Electrical Characteristics** for details on the measurement conditions.

1.2 Product List

Table 1.3 lists Product List for R8C/3MQ Group. Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/3MQ Group.

Table 1.3 Product List for R8C/3MQ Group **Current of Aug 2011**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F213M6QNNP	32 Kbytes	1 Kbyte × 4	2.5 Kbytes	PWQN0040KB-A	N version
R5F213M7QNNP	48 Kbytes	1 Kbyte × 4	4 Kbytes		
R5F213M8QNNP	64 Kbytes	1 Kbyte × 4	6 Kbytes		
R5F213MAQNNP	96 Kbytes	1 Kbyte × 4	7 Kbytes		
R5F213MCQNNP	128 Kbytes	1 Kbyte × 4	7.5 Kbytes		

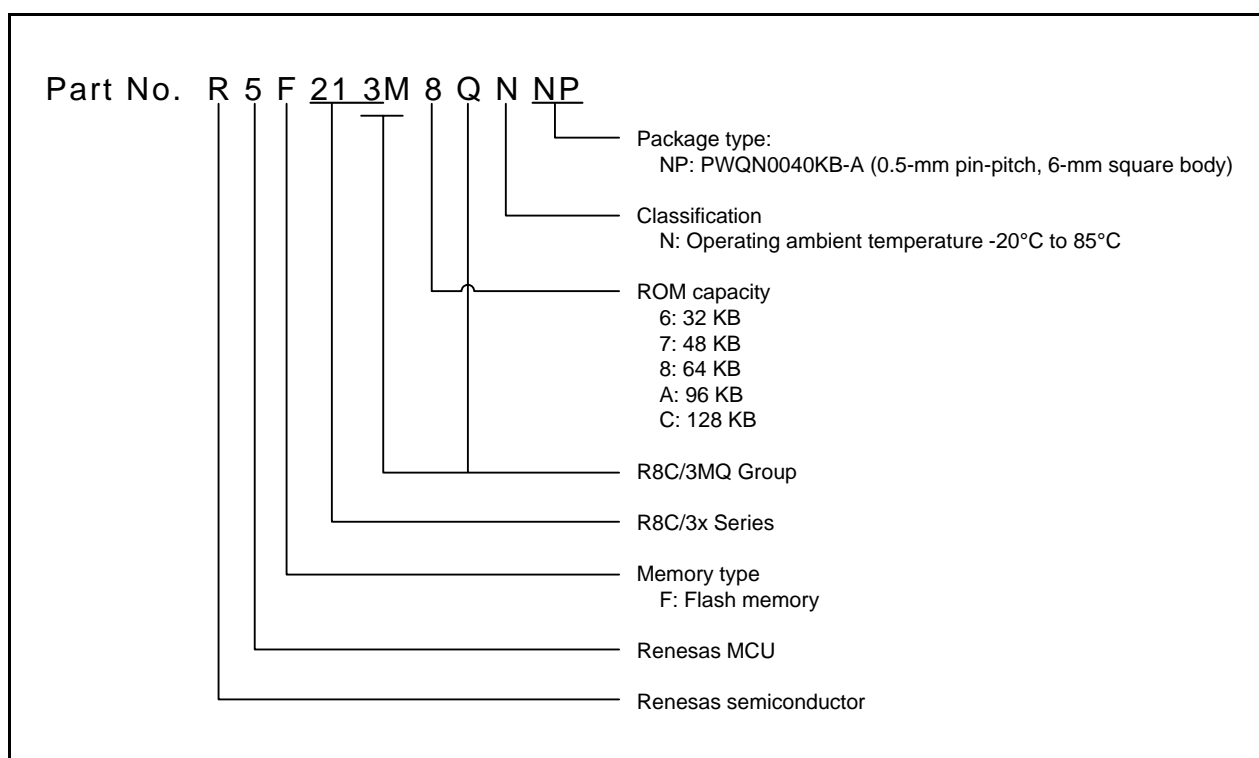


Figure 1.1 Part Number, Memory Size, and Package of R8C/3MQ Group

1.3 Block Diagram

Figure 1.2 shows a Block Diagram.

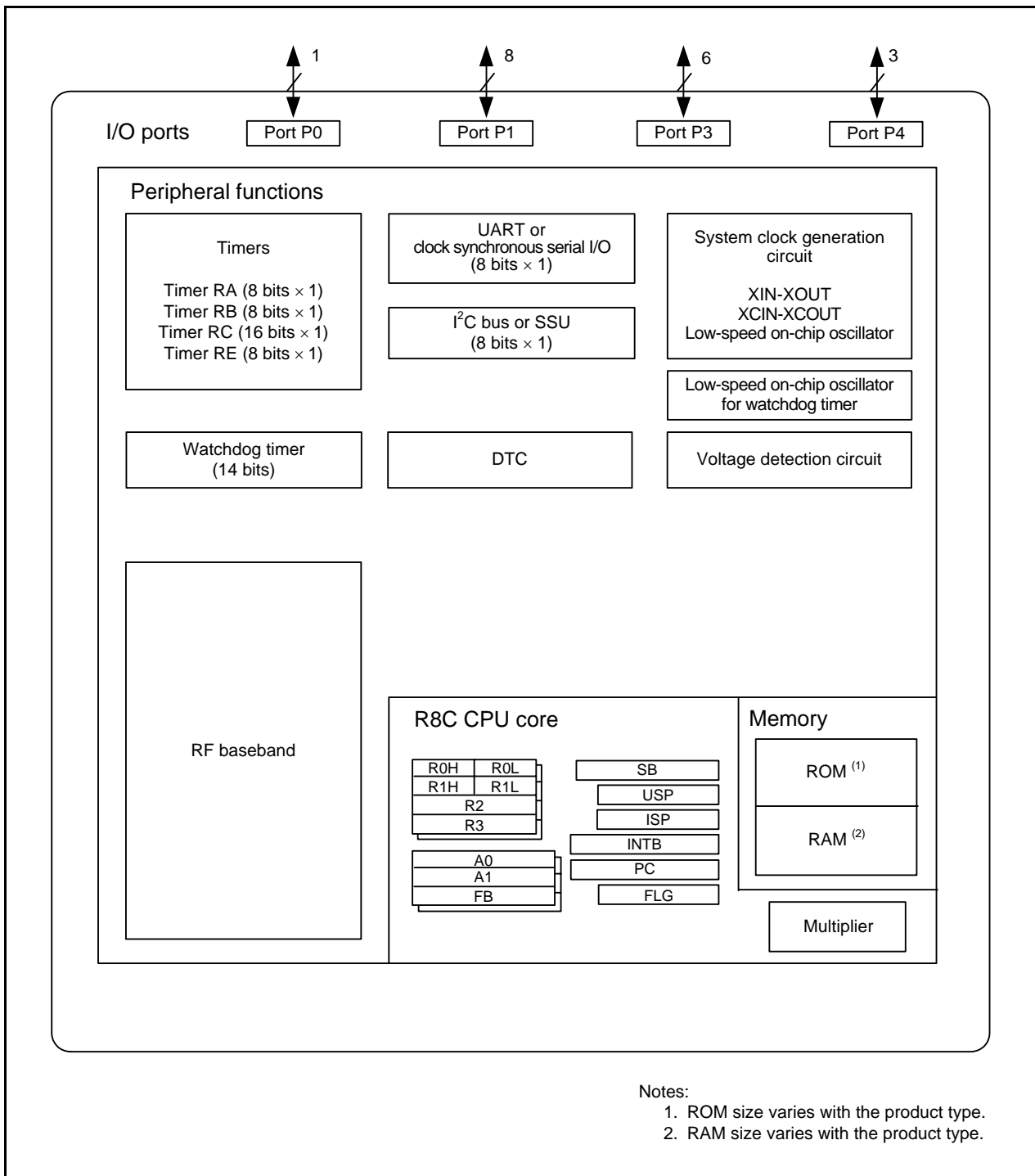


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Table 1.4 outlines Pin Name Information by Pin Number.

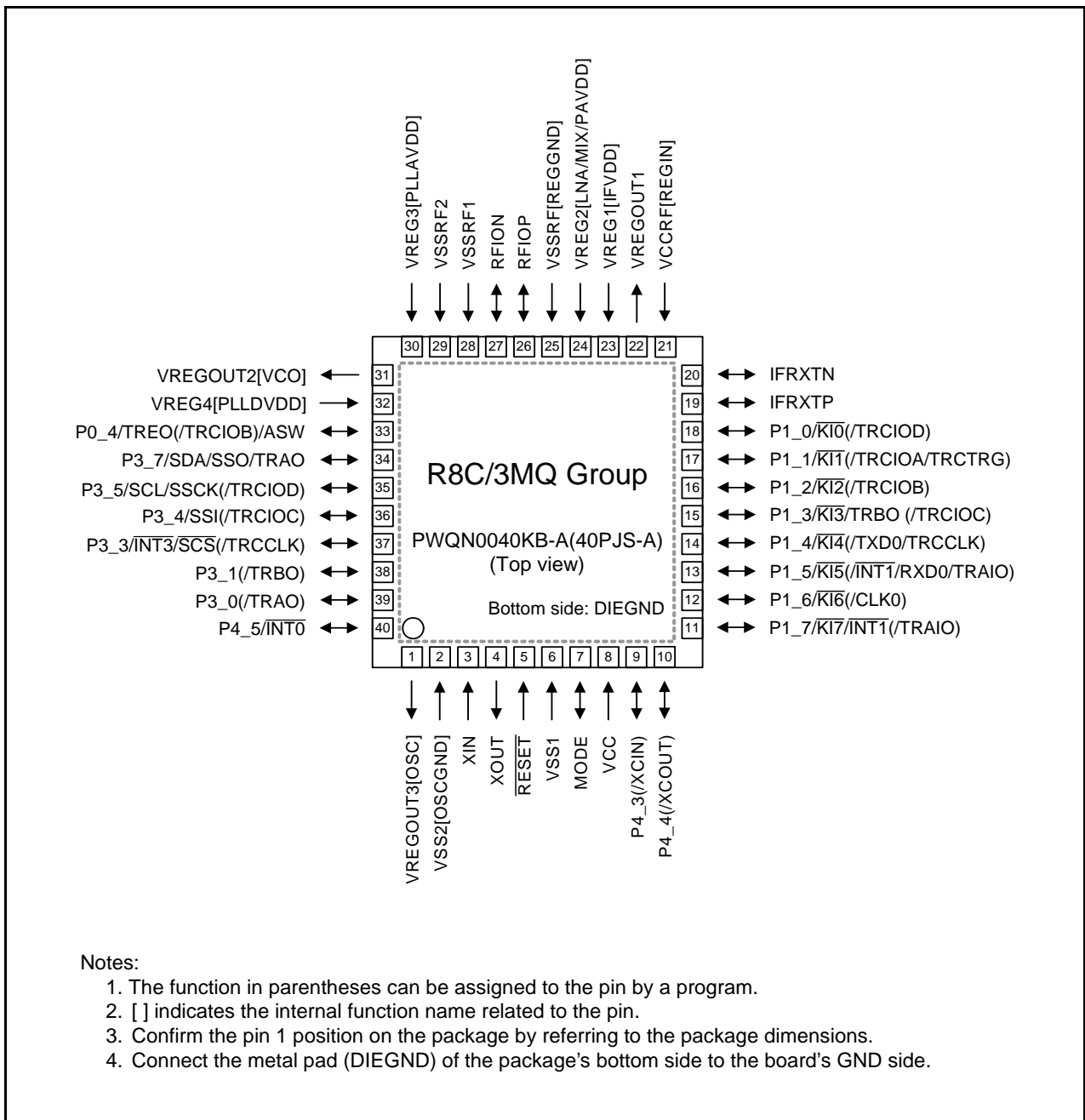


Figure 1.3 Pin Assignment (Top View)

Table 1.4 Pin Name Information by Pin Number

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I ² C bus	RF Pin Other
1	VREGOUT3							
2	VSS2							
3	XIN							
4	XOUT							
5	RESET							
6	VSS1							
7	MODE							
8	VCC							
9	(XCIN)	P4_3						
10	(XCOUT)	P4_4						
11		P1_7	$\overline{KI7}/\overline{INT1}$	(TRAIO)				
12		P1_6	$\overline{KI6}$		(CLK0)			
13		P1_5	$\overline{KI5}/\overline{INT1}$	(TRAIO)	(RXD0)			
14		P1_4	$\overline{KI4}$	(TRCCLK)	(TXD0)			
15		P1_3	$\overline{KI3}$	TRBO(/TRCIOC)				
16		P1_2	$\overline{KI2}$	(TRCIOB)				
17		P1_1	$\overline{KI1}$	(TRCIOA/TRCTRG)				
18		P1_0	$\overline{KI0}$	(TRCIOD)				
19								IFRXTP
20								IFRXTN
21	VCCRF							
22	VREGOUT1							
23	VREG1							
24	VREG2							
25	VSSRF							
26								RFIOP
27								RFION
28	VSSRF1							
29	VSSRF2							
30	VREG3							
31	VREGOUT2							
32	VREG4							
33		P0_4		TREO(/TRCIOB)				ASW
34		P3_7		TRAO		SSO	SDA	
35		P3_5		(TRCIOD)		SSCK	SCL	
36		P3_4		(TRCIOC)		SSI		
37		P3_3	$\overline{INT3}$	(TRCCLK)		\overline{SCS}		
38		P3_1		(TRBO)				
39		P3_0		(TRAO)				
40		P4_5	$\overline{INT0}$					
Bottom side	DIEGND							

Note:

1. The function in parentheses can be assigned to the pin by a program.

1.5 Pin Functions

Tables 1.5 and 1.6 list Pin Functions.

Table 1.5 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS1	—	Apply 1.8 to 3.6 V to the VCC pin. Apply 0 V to the VSS1 pin.
Reset input	$\overline{\text{RESET}}$	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock oscillation circuit I/O. Connect a crystal oscillator between the XIN and XOUT pins.
XIN clock output	XOUT	I/O	
XCIN clock input	XCIN	I	These pins are provided for XCIN clock oscillation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT pins.
XCIN clock output	XCOUT	O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is used as an input pin for timer RB and timer RC.
Key input interrupt input	$\overline{\text{KI0}}$ to $\overline{\text{KI7}}$	I	Key input interrupt input pins.
Timer RA	TRAIO	I/O	Timer RA I/O pin.
	TRAO	O	Timer RA output pin.
Timer RB	TRBO	O	Timer RB output pin.
Timer RC	TRCCLK	I	External clock input pin.
	TRCTRG	I	External trigger input pin.
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins.
Timer RE	TREO	O	Divided clock output pin.
Serial interface	CLK0	I/O	Transfer clock I/O pin.
	RXD0	I	Serial data input pin.
	TXD0	O	Serial data output pin.
SSU	SSI	I/O	Data I/O pin.
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin.
	SSCK	I/O	Clock I/O pin.
	SSO	I/O	Data I/O pin.
I ² C bus	SCL	I/O	Clock I/O pin
	SDA	I/O	Data I/O pin
I/O ports	P0_4, P1_0 to P1_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program.

I: Input O: Output I/O: Input and output

Table 1.6 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Analog power supply input	VCCRF, VSSRF, VSSRF1, VSSRF2, VSS2, DIEGND	—	Apply the same voltage as the VCC of 1.8 V to 3.6 V to VCCRF. Apply 0 V to VSSRF, VSSRF1, VSSRF2, VSS2, and DIEGND.
	VREG1	—	1.5 V IF VDD pin. Connect to the VREGOUT1 pin.
	VREG2	—	1.5 V LNA/MIX/PA VDD pin. Connect to the VREGOUT1 pin.
	VREG3	—	1.5 V PLL ANALOG VDD pin. Connect to the VREGOUT1 pin.
	VREG4	—	1.5 V PLL DIGITAL VDD pin. Connect to the VREGOUT1 pin.
Regulator output	VREGOUT1	—	On-chip regulator output (1.5 V) pin for the analog circuit. Connect only a bypass capacitor between pins VREGOUT1 and VSS. Use only as the power supply for pins VREG1, VREG2, VREG3, and VREG4.
	VREGOUT2	—	Regulator output (1.5 V) pin for the VCO circuit. Connect only a bypass capacitor between pins VREGOUT2 and VSS. Do not use as the power supply for other circuits.
	VREGOUT3	—	Regulator output (1.5 V) pin for the XIN oscillation circuit. Connect only a bypass capacitor between pins VREGOUT3 and VSS. Do not use as the power supply for other circuits.
RF I/O	RFIOP, RFION	I/O	RF I/O pins
Test pins	IFRXTN, IFRXTP	I/O	Ports for testing. Leave open or apply 0 V.
External antenna switch control output	ASW	O	Signal output pin to control the external antenna switch. If antenna switch control is not required, leave open.

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

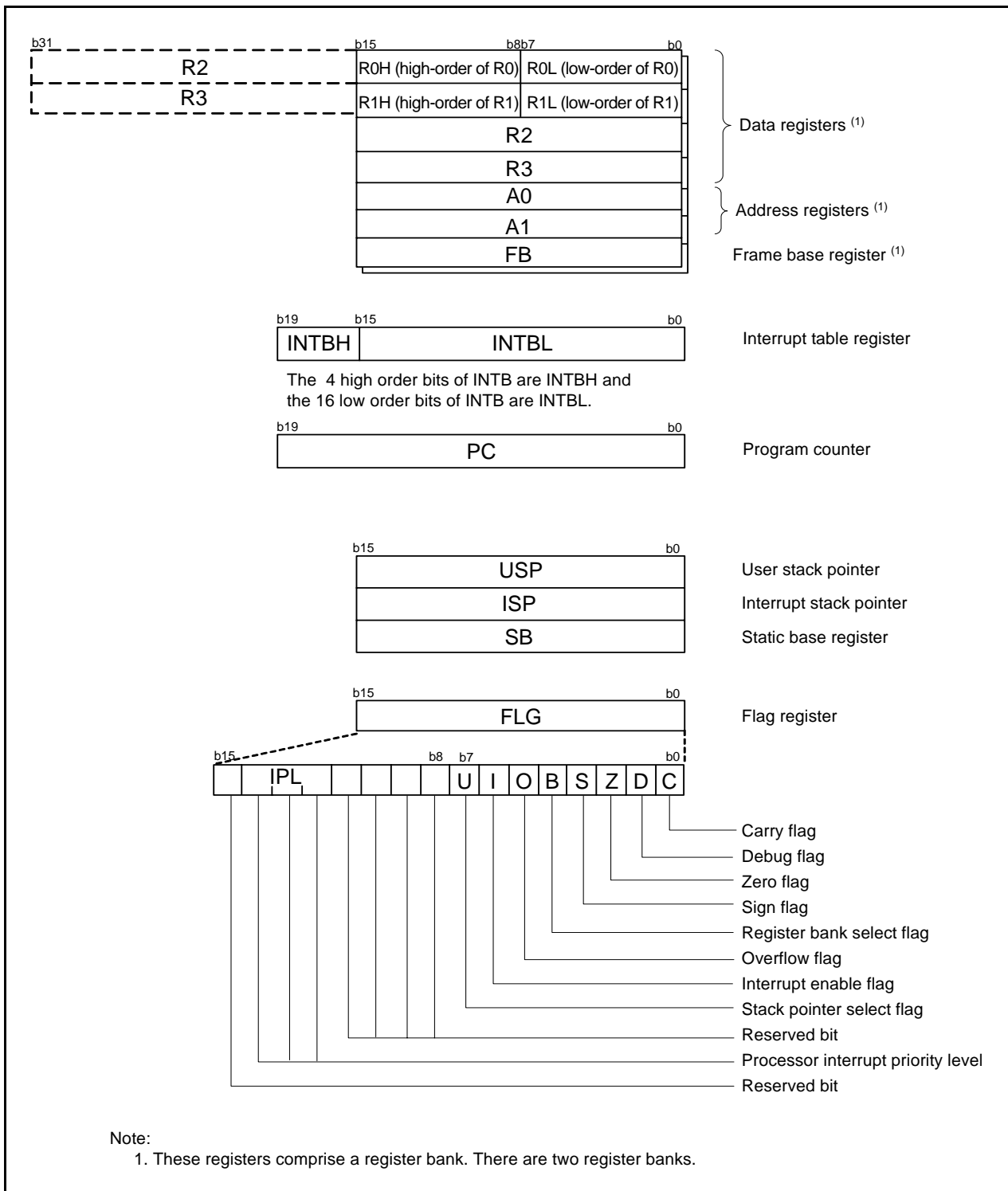


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/3MQ Group

Figure 3.1 is a Memory Map of R8C/3MQ Group. The R8C/3MQ Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. However, for products with internal ROM (program ROM) capacity of 64 Kbytes or more, the internal ROM is also allocated higher addresses, beginning with address 0FFFFh.

For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh, and a 96-Kbyte internal ROM is allocated addresses 04000h to 1BFFFh.

The fixed interrupt vector table is allocated addresses 08000h to 0FFFFh. The starting address of each interrupt routine is stored here.

The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.

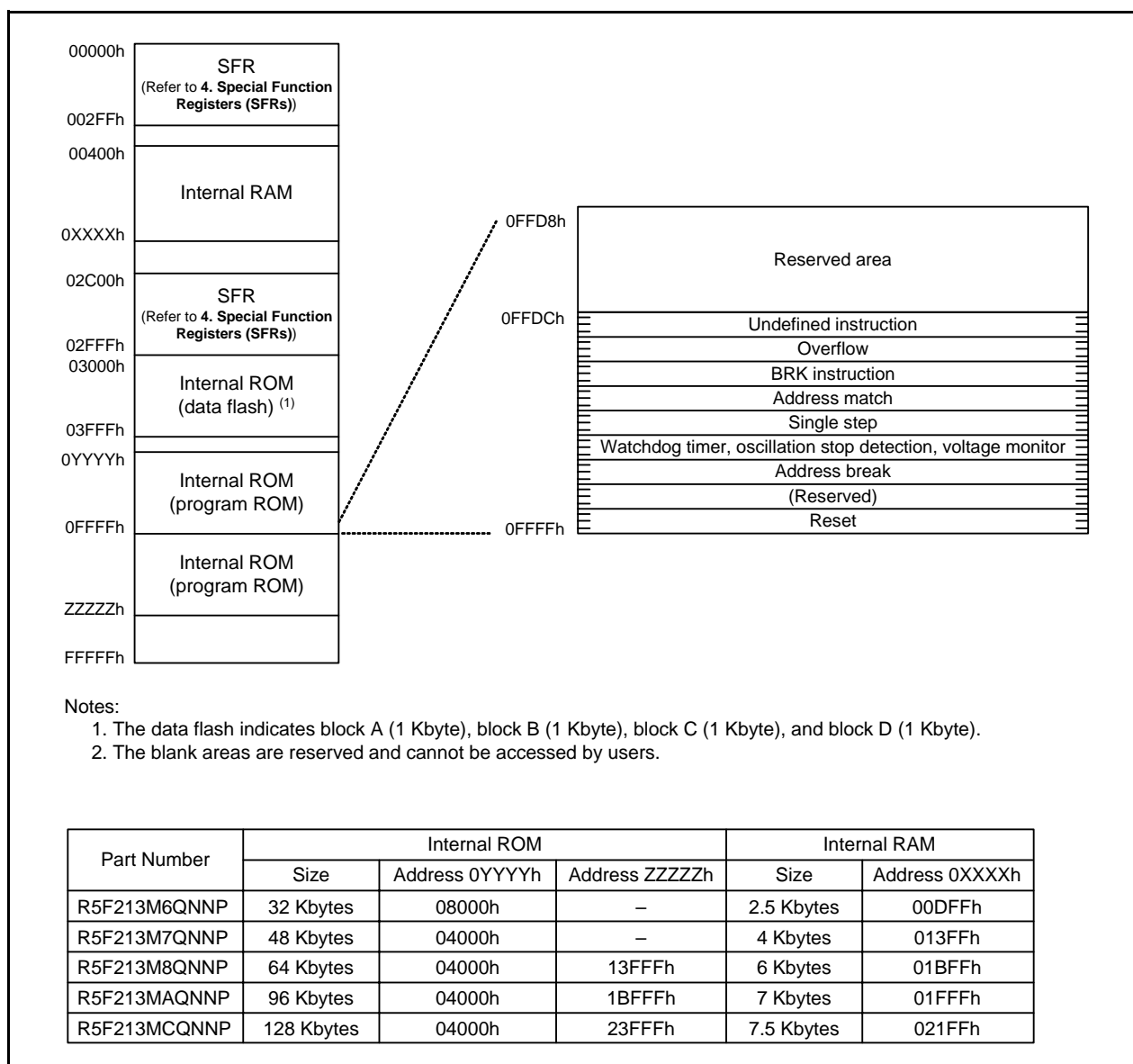


Figure 3.1 Memory Map of R8C/3MQ Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.11 list the special function registers. Table 4.12 lists the ID Code Areas and Option Function Select Area.

Table 4.1 SFR Information (1) (0000h to 002Fh) (1)

Address	Register	Symbol	After Reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	00101000b
0007h	System Clock Control Register 1	CM1	00101000b
0008h	Module Standby Control Register	MSTCR	00h
0009h	System Clock Control Register 3	CM3	00h
000Ah	Protect Register	PRCR	00h
000Bh	Reset Source Determination Register	RSTFR	0XXXXXXXXb (2)
000Ch	Oscillation Stop Detection Register	OSD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDTC	00111111b
0010h			
0011h			
0012h			
0013h			
0014h			
0015h			
0016h			
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b (3)
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. The CWR bit in the RSTFR register is set to 0 after power-on and voltage monitor 0 reset. Hardware reset, software reset, or watchdog timer reset does not affect this bit.
3. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2) (0030h to 006Fh) (1)

Address	Register	Symbol	After Reset
0030h	Voltage Monitor Circuit Control Register	CMPA	00h
0031h	Voltage Monitor Circuit Edge Select Register	VCAC	00h
0032h			
0033h			
0034h	Voltage detection Register 2	VCA2	00h ⁽³⁾ 00100000b ⁽⁴⁾
0035h			
0036h	Voltage Detection 1 Level Select Register	VD1LS	00000111b
0037h			
0038h	Voltage Monitor 0 Circuit Control Register	VW0C	1100X010b ⁽³⁾ 1100X011b ⁽⁴⁾
0039h	Voltage Monitor 1 Circuit Control Register	VW1C	10001010b
003Ah	WDT Detection Flag	VW2C	1000010b
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
0040h			
0041h	Flash Memory Ready Interrupt Control Register	FMRDYIC	XXXXX000b
0042h	BB Timer Compare 2 Interrupt Control Register	BBTIM2IC	XXXXX000b
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh			
004Fh	SSU Interrupt Control Register/IIC bus Interrupt Control Register ⁽²⁾	SSUIC/IICIC	XXXXX000b
0050h			
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h			
0054h	Bank 0 Reception Complete/IDLE Interrupt Control Register ⁽⁵⁾	BBRX0IC/BBIDELIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h			
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh			
005Ch	BB Timer Compare 1 Interrupt Control Register	BBTIM1IC	XX00X000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh	CCA Complete Interrupt Control Register	BBCCAIC	XXXXX000b
005Fh	BB Timer Compare 0 Interrupt Control Register	BBTIM0IC	XXXXX000b
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch	Address Filter Interrupt Control Register	BBADFIC	XXXXX000b
006Dh	Transmit Overrun Interrupt Control Register	BBTXORIC	XXXXX000b
006Eh	Transmission Complete Interrupt Control Register	BBTXIC	XX00XX00b
006Fh	Receive Overrun 1 Interrupt Control Register	BBRXOR1IC	XXXXX000b

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.
3. The LVDAS bit in the OFS register is set to 1.
4. The LVDAS bit in the OFS register is set to 0.
5. Can be selected by the BANK0INTSEL bit in the BBTXRXMODE4 register.

Table 4.3 SFR Information (3) (0070h to 00AFh) (1)

Address	Register	Symbol	After Reset
0070h	PLL Lock Detection Interrupt Control Register	BBPLLIC	XXXXX000b
0071h	Receive Overrun 0/Calibration Complete Interrupt Control Register (3)	BBRXOR0IC/BBCALIC	XXXXX000b
0072h	Voltage Monitor 1 Interrupt Control Register	VCMP1IC	XXXXX000b
0073h	Bank 1 Reception Complete/Clock Regulator Interrupt Control Register (2)	BBRX1IC/BBCREGIC	XXXXX000b
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			
0080h	DTC Activation Control Register	DTCTL	00h
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h	DTC Activation Enable Register 0	DTCEN0	00h
0089h	DTC Activation Enable Register 1	DTCEN1	00h
008Ah	DTC Activation Enable Register 2	DTCEN2	00h
008Bh	DTC Activation Enable Register 3	DTCEN3	00h
008Ch			
008Dh	DTC Activation Enable Register 5	DTCEN5	00h
008Eh	DTC Activation Enable Register 6	DTCEN6	00h
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh			
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h	UART0 Transmit/Receive Control Register 1	U0C1	00000010b
00A6h	UART0 Receive Buffer Register	U0RB	XXh
00A7h			XXh
00A8h			
00A9h			
00AAh			
00ABh			
00ACh			
00ADh			
00AEh			
00AFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Can be selected by the BANK1INTSEL bit in the BBTXRXMODE4 register.
3. Can be selected by the ROR0INTSEL bit in the BBTXRXMODE4 register.

Table 4.4 SFR Information (4) (00B0h to 011Fh) (1)

Address	Register	Symbol	After Reset
00B0h			
:			
00DFh			
00DFh			
00E0h	Port P0 Register	P0	XXh
00E1h	Port P1 Register	P1	XXh
00E2h	Port P0 Direction Register	PD0	00h
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh			
00FDh			
00FEh			
00FFh			
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h			
0107h			
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRES	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh			
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
011Ah	Timer RE Hour Data Register	TREHR	00h
011Bh	Timer RE Day of Week Data Register	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.5 SFR Information (5) (0120h to 019Fh) (1)

Address	Register	Symbol	After Reset
0120h	Timer RC Mode Register	TRCMR	01001000b
0121h	Timer RC Control Register 1	TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h			00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h			FFh
012Ah	Timer RC General Register B	TRCGRB	FFh
012Bh			FFh
012Ch	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh
012Eh	Timer RC General Register D	TRCGRD	FFh
012Fh			FFh
0130h	Timer RC Control Register 2	TRCCR2	00011000b
0131h	Timer RC Digital Filter Function Select Register	TRCDF	00h
0132h	Timer RC Output Master Enable Register	TRCOER	01111111b
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
:			
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h			
0185h			
0186h			
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h			
018Ah			
018Bh			
018Ch	SSU/IIC Pin Select Register	SSUICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUICSR register.

Table 4.6 SFR Information (6) (01A0h to 02FFh) (1)

Address	Register	Symbol	After Reset
01A0h			
:			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			
01C0h	Address Match Interrupt Register 0	RMAD0	XXh
01C1h			XXh
01C2h			0000XXXXb
01C3h	Address Match Interrupt Enable Register 0	AIER0	00h
01C4h	Address Match Interrupt Register 1	RMAD1	XXh
01C5h			XXh
01C6h			0000XXXXb
01C7h	Address Match Interrupt Enable Register 1	AIER1	00h
01C8h			
:			
01DFh			
01E0h	Pull-Up Control Register 0	PUR0	00h
01E1h	Pull-Up Control Register 1	PUR1	00h
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Port P1 Drive Capacity Control Register	P1DRR	00h
01F1h			
01F2h	Drive Capacity Control Register 0	DRR0	00h
01F3h	Drive Capacity Control Register 1	DRR1	00h
01F4h			
01F5h	Input Threshold Control Register 0	VLT0	00h
01F6h	Input Threshold Control Register 1	VLT1	00h
01F7h			
01F8h			
01F9h			
01FAh	External Input Enable Register 0	INTEN	00h
01FBh			
01FCh	INT Input Filter Select Register 0	INTF	00h
01FDh			
01FEh	Key Input Enable Register 0	KIEN	00h
01FFh	Key Input Enable Register 1	KI1EN	00h
0200h			
:			
02FFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.7 SFR Information (7) (2C00h to 2C6Fh) (1)

Address	Register	Symbol	After Reset
2C00h	DTC Transfer Vector Area		XXh
2C01h	DTC Transfer Vector Area		XXh
2C02h	DTC Transfer Vector Area		XXh
2C03h	DTC Transfer Vector Area		XXh
2C04h	DTC Transfer Vector Area		XXh
2C05h	DTC Transfer Vector Area		XXh
2C06h	DTC Transfer Vector Area		XXh
2C07h	DTC Transfer Vector Area		XXh
2C08h	DTC Transfer Vector Area		XXh
2C09h	DTC Transfer Vector Area		XXh
2C0Ah	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
:	DTC Transfer Vector Area		XXh
2C3Ah	DTC Transfer Vector Area		XXh
2C3Bh	DTC Transfer Vector Area		XXh
2C3Ch	DTC Transfer Vector Area		XXh
2C3Dh	DTC Transfer Vector Area		XXh
2C3Eh	DTC Transfer Vector Area		XXh
2C3Fh	DTC Transfer Vector Area		XXh
2C40h	DTC Control Data 0	DTCD0	XXh
2C41h			XXh
2C42h			XXh
2C43h			XXh
2C44h			XXh
2C45h			XXh
2C46h			XXh
2C47h			XXh
2C48h	DTC Control Data 1	DTCD1	XXh
2C49h			XXh
2C4Ah			XXh
2C4Bh			XXh
2C4Ch			XXh
2C4Dh			XXh
2C4Eh			XXh
2C4Fh			XXh
2C50h	DTC Control Data 2	DTCD2	XXh
2C51h			XXh
2C52h			XXh
2C53h			XXh
2C54h			XXh
2C55h			XXh
2C56h			XXh
2C57h			XXh
2C58h	DTC Control Data 3	DTCD3	XXh
2C59h			XXh
2C5Ah			XXh
2C5Bh			XXh
2C5Ch			XXh
2C5Dh			XXh
2C5Eh			XXh
2C5Fh			XXh
2C60h	DTC Control Data 4	DTCD4	XXh
2C61h			XXh
2C62h			XXh
2C63h			XXh
2C64h			XXh
2C65h			XXh
2C66h			XXh
2C67h			XXh
2C68h	DTC Control Data 5	DTCD5	XXh
2C69h			XXh
2C6Ah			XXh
2C6Bh			XXh
2C6Ch			XXh
2C6Dh			XXh
2C6Eh			XXh
2C6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.8 SFR Information (8) (2C70h to 2CAfh) (1)

Address	Register	Symbol	After Reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.9 SFR Information (9) (2CB0h to 2CEFh) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.10 SFR Information (10) (2CF0h to 2D2Fh) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h	Baseband Control Register	BBCON	00h
2D01h	Transmit/Receive Reset Register	BBTXRXRST	00h
2D02h	Transmit/Receive Mode Register 0	BBTXRXMODE0	00h
2D03h	Transmit/Receive Mode Register 1	BBTXRXMODE1	00h
2D04h	Receive Frame Length Register	BBRXFLEN	00h
2D05h	Receive Data Counter Register	BBRXCOUNT	00h
2D06h	RSSI/CCA Result Register	BBRSSICCARSLT	00h
2D07h	Transmit/Receive Status Register 0	BBTXRXST0	80h
2D08h	Transmit Frame Length Register	BBTXFLEN	00h
2D09h	Transmit/Receive Mode Register 2	BBTXRXMODE2	30h
2D0Ah	Transmit/Receive Mode Register 3	BBTXRXMODE3	00h
2D0Bh	Receive Level Threshold Set Register	BBLVLVTH	80h
2D0Ch	Transmit/Receive Control Register	BBTXRXCON	00h
2D0Dh	CSMA Control Register 0	BBCSMACON0	00h
2D0Eh	CCA Level Threshold Set Register	BBCCAVTH	80h
2D0Fh	Transmit/Receive Status Register 1	BBTXRXST1	00h
2D10h	RF Control Register	BBRFCON	00h
2D11h	Transmit/Receive Mode Register 4	BBTXRXMODE4	00h
2D12h	CSMA Control Register 1	BBCSMACON1	9Ch
2D13h	CSMA Control Register 2	BBCSMACON2	05h
2D14h	PAN Identifier Register	BBPANID	00h
2D15h			00h
2D16h	Short Address Register	BBSHORTAD	00h
2D17h			00h
2D18h	Extended Address Register	BBEXTENDAD0	00h
2D19h			00h
2D1Ah		BBEXTENDAD1	00h
2D1Bh			00h
2D1Ch		BBEXTENDAD2	00h
2D1Dh			00h
2D1Eh		BBEXTENDAD3	00h
2D1Fh			00h
2D20h	Timer Read-Out Register 0	BBTIMEREAD0	00h
2D21h			00h
2D22h	Timer Read-Out Register 1	BBTIMEREAD1	00h
2D23h			00h
2D24h	Timer Compare 0 Register 0	BBCOMP0REG0	00h
2D25h			00h
2D26h	Timer Compare 0 Register 1	BBCOMP0REG1	00h
2D27h			00h
2D28h	Timer Compare 1 Register 0	BBCOMP1REG0	00h
2D29h			00h
2D2Ah	Timer Compare 1 Register 1	BBCOMP1REG1	00h
2D2Bh			00h
2D2Ch	Timer Compare 2 Register 0	BBCOMP2REG0	00h
2D2Dh			00h
2D2Eh	Timer Compare 2 Register 1	BBCOMP2REG1	00h
2D2Fh			00h

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (2D30h to 2FFFh) (1)

Address	Register	Symbol	After Reset
2D30h	Time Stamp Register 0	BBTSTAMP0	00h
2D31h			00h
2D32h	Time Stamp Register 1	BBTSTAMP1	00h
2D33h			00h
2D34h	Timer Control Register	BBTIMECON	00h
2D35h	Backoff Period Register	BBBOFFPROD	00h
2D36h			
2D37h			
2D38h			
2D39h			
2D3Ah	PLL Division Register 0	BBPLLDIVL	65h
2D3Bh	PLL Division Register 1	BBPLLDIVH	09h
2D3Ch	Transmit Output Power Register	BBTXOUTPWR	00h
2D3Dh	RSSI Offset Register	BBRSSIOFS	F6h
2D3Eh			
2D3Fh			
2D40h			
:			
2D45h			
2D46h	Automatic ACK Response Timing Adjustment Register	BBACKRTNTIMG	22h
2D47h			
:			
2D63h			
2D64h			
2D65h			
2D66h			
2D67h			
2D68h	Verification Mode Set Register	BBEVAREG	00h
2D69h			
2D6Ah			
2D6Bh			
2D6Ch			
2D6Dh			
2D6Eh			
2D6Fh			
2D70h			
2D71h			
2D72h			
2D73h			
2D74h			
2D75h			
2D76h	IDLE Wait Set Register	BBIDELWAIT	01h
2D77h			
2D78h			
2D79h			
2D7Ah	ANTSW Output Timing Set Register	BBANTSWTIMG	72h
2D7Bh			
2D7Ch	RF Initial Set Register	BBRFINI	XXh
2D7Dh			XXh
2D7Eh			
2D7Fh			
2D80h			
2D81h			
2D82h	ANTSW Control Register	BBANTSWCON	00h
2D83h			
:			
2DFFh			
2E00h	Transmit RAM	TRANSMIT_RAM_START	
:	Transmit RAM		
2E7Eh	Transmit RAM	TRANSMIT_RAM_END	
2E7Fh			
2D80h	Receive RAM	RECIEVE_RAM_START	
:	Receive RAM		
2EFEh	Receive RAM	RECIEVE_RAM_END	
2EFFh			
2F00h			
:			
2FFFh			

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
⋮			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
⋮			
FFDFh	ID1		(Note 2)
⋮			
FFE3h	ID2		(Note 2)
⋮			
FFEBh	ID3		(Note 2)
⋮			
FFEFh	ID4		(Note 2)
⋮			
FFF3h	ID5		(Note 2)
⋮			
FFF7h	ID6		(Note 2)
⋮			
FFFBh	ID7		(Note 2)
⋮			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:

- The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
At shipment, the option function select area is set to FFh. It is set to the written value after written by the user.
- The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
At shipment, the ID code areas are set to FFh. They are set to the written value after written by the user.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Rated Value	Unit
VCC	Digital supply voltage			-0.3 to 3.8	V
VCCRF	Analog supply voltage			-0.3 to 3.8	V
Vi	Input voltage	RESET, MODE, P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5		-0.3 to Vcc + 0.3	V
Vo	Output voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5		-0.3 to Vcc + 0.3	V
VRFIO	RF I/O pins	RFIOP, RFION		-0.3 to 2.1	V
VTESTIO	Test ports	IFRXTN, IFRXTP		-0.3 to 2.1	V
VANAIN	1.5 V analog supply (input)	VREG1, VREG2, VREG3, VREG4		-0.3 to 2.1	V
VANAOUT	1.5 V analog supply (output)	VREGOUT1, VREGOUT2, VREGOUT3		-0.3 to 2.1	V
VXINOUT	Main clock I/O	XIN, XOUT		-0.3 to 2.1	V
Pd	Power dissipation		-20°C ≤ Topr ≤ 85°C	300	mW
Topr	Operating ambient temperature	(1) During MCU operation under the conditions other than (2) and (3) below.		-20 to 85	°C
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.		0 to 60	
		(3) During on-chip debugging with the E8a emulator connected		10 to 35	
Tstg	Storage temperature			-65 to 150	°C

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter		Conditions	Standard			Unit		
				Min.	Typ.	Max.			
VCC	Digital supply voltage	(1) During MCU operation under the conditions other than (2) and (3) below.		1.8	3.3	3.6	V		
		(2) During programming and erasing of the flash memory using a serial programmer or parallel programmer.		2.7	—	3.6			
		(3) During on-chip debugging with the E8a emulator connected		2.7	—	3.6			
VCCRF	Analog supply voltage			1.8	3.3	3.6	V		
VSS/ VSS2/ VSSRF/ VSSRF1/ VSSRF2/ DIEGND	Supply voltage	VSS1, VSS2, VSSRF, VSSRF1, VSSRF2, DIEGND		—	0	—	V		
VIH	Input "H" voltage	Other than CMOS input			0.8 Vcc	—	Vcc	V	
		CMOS input	Input level switching function (I/O port)	Input level selection: 2.7 V ≤ Vcc ≤ 3.6 V	0.55 Vcc	—	Vcc	V	
				0.35 Vcc	1.8 V ≤ Vcc < 2.7 V	0.65 Vcc	—	Vcc	V
				Input level selection: 2.7 V ≤ Vcc ≤ 3.6 V	0.7 Vcc	—	Vcc	V	
				0.5 Vcc	1.8 V ≤ Vcc < 2.7 V	0.8 Vcc	—	Vcc	V
Input level selection: 2.7 V ≤ Vcc ≤ 3.6 V	0.85 Vcc	—	Vcc	V					
0.7 Vcc	1.8 V ≤ Vcc < 2.7 V	0.85 Vcc	—	Vcc	V				
VIL	Input "L" voltage	Other than CMOS input			0	—	0.2 Vcc	V	
		CMOS input	Input level switching function (I/O port)	Input level selection: 2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.2 Vcc	V	
				0.35 Vcc	1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
				Input level selection: 2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.3 Vcc	V	
				0.5 Vcc	1.8 V ≤ Vcc < 2.7 V	0	—	0.2 Vcc	V
Input level selection: 2.7 V ≤ Vcc ≤ 3.6 V	0	—	0.45 Vcc	V					
0.7 Vcc	1.8 V ≤ Vcc < 2.7 V	0	—	0.35 Vcc	V				
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)			—	—	-160	mA	
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)			—	—	-80	mA	
IOH(peak)	Peak output "H" current	Drive capacity Low			—	—	-10	mA	
		Drive capacity High			—	—	-40	mA	
IOH(avg)	Average output "H" current	Drive capacity Low			—	—	-5	mA	
		Drive capacity High			—	—	-20	mA	
IOI(sum)	Peak sum output "L" current	Sum of all pins IOI(peak)			—	—	160	mA	
IOI(sum)	Average sum output "L" current	Sum of all pins IOI(avg)			—	—	80	mA	
IOI(peak)	Peak output "L" current	Drive capacity Low			—	—	10	mA	
		Drive capacity High			—	—	40	mA	
IOI(avg)	Average output "L" current	Drive capacity Low			—	—	5	mA	
		Drive capacity High			—	—	20	mA	
f(XIN)	XIN clock input oscillation frequency		1.8 V ≤ Vcc ≤ 3.6 V	—	16	—	MHz		
f(XCIN)	XCIN clock input oscillation frequency		1.8 V ≤ Vcc ≤ 3.6 V	30	32.768	35	kHz		
—	System clock frequency	f(XIN)=16 MHz	1.8 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz		
f(BCLK)	CPU clock frequency	f(XIN)=16 MHz	2.7 V ≤ Vcc ≤ 3.6 V	—	—	16	MHz		
			2.2 V ≤ Vcc < 2.7 V	—	—	8			
			1.8 V ≤ Vcc < 2.2 V	—	—	4			

Notes:

1. Vcc = 1.8 to 3.6 V and T_{opr} = -20°C to 85°C, unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

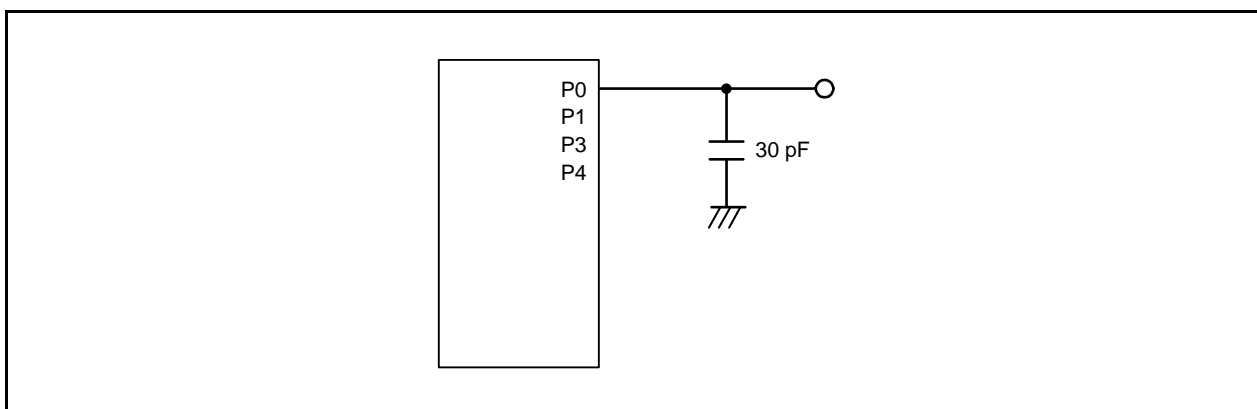


Figure 5.1 Ports P0, P1, P3 and P4 Timing Measurement Circuit

Table 5.3 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		1,000 ⁽³⁾	—	—	times
—	Byte program time		—	80	500	μs
—	Block erase time		—	0.3	—	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature		0	—	60	°C
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

1. V_{CC} = 2.7 to 3.6 V and T_{opr} = 0 to 60°C, unless otherwise specified.
2. Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.4 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance ⁽²⁾		10,000 ⁽³⁾	—	—	times
—	Byte program time (program/erase endurance ≤ 1,000 times)		—	160	1500	μs
—	Byte program time (program/erase endurance > 1,000 times)		—	300	1500	μs
—	Block erase time (program/erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (program/erase endurance > 1,000 times)		—	0.3	1	s
t _d (SR-SUS)	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	μs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	μs
t _d (CMDRST-READY)	Time from when command is forcibly stopped until reading is enabled		—	—	30 + CPU clock × 1 cycle	μs
—	Program, erase voltage	CPU rewrite mode	1.8	—	3.6	V
		Standard serial I/O mode	2.7	—	3.6	
		Parallel I/O mode	2.7	—	3.6	
—	Read voltage		1.8	—	3.6	V
—	Program, erase temperature	CPU rewrite mode	-20	—	85	°C
		Standard serial I/O mode	0	—	60	
		Parallel I/O mode	0	—	60	
—	Data hold time ⁽⁷⁾	Ambient temperature = 55°C	20	—	—	year

Notes:

- V_{CC} = 1.8 to 3.6 V and T_{opr} = -20°C to 85°C, unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed.)
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

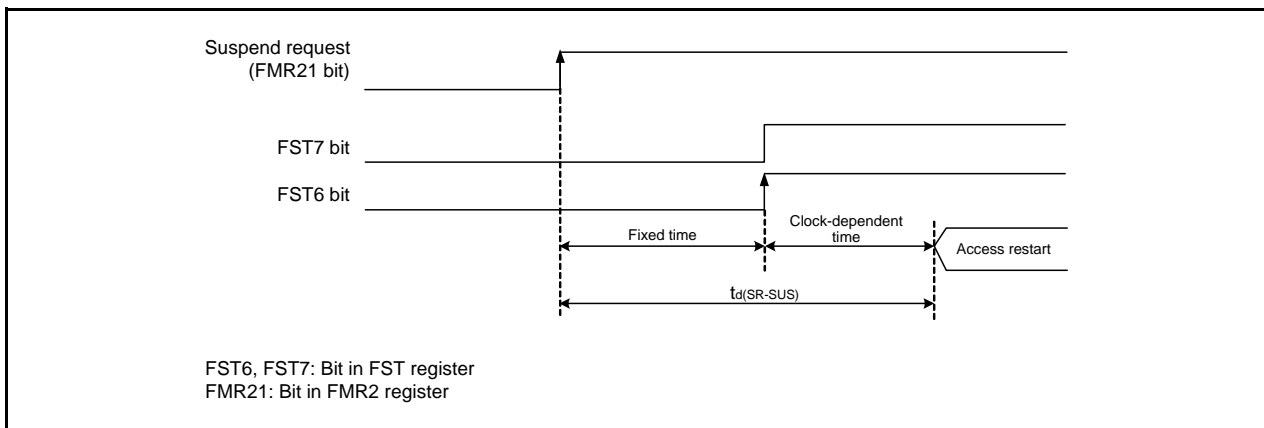


Figure 5.2 Time delay until Suspend

Table 5.5 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det0}	Voltage detection level V _{det0_0}		1.80	1.90	2.05	V
—	Voltage detection 0 circuit response time ⁽³⁾	At the falling of V _{CC} from 3.6 V to (V _{det0_0} – 0.1) V	—	6	150	μs
—	Voltage detection circuit self power consumption	VCA25 = 1, V _{CC} = 3.0 V	—	1.5	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽²⁾		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
3. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.6 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{det1}	Voltage detection level V _{det1_2} ⁽²⁾	At the falling of V _{CC}	2.30	2.50	2.70	V
	Voltage detection level V _{det1_5} ⁽²⁾	At the falling of V _{CC}	2.75	2.95	3.15	V
—	Hysteresis width at the rising of V _{CC} in voltage detection 1 circuit		—	0.07	—	V
—	Voltage detection 1 circuit response time ⁽³⁾	At the falling of V _{CC} from 3.6 V to (V _{det1_0} – 0.1) V	—	60	150	μs
—	Voltage detection circuit self power consumption	VCA26 = 1, V _{CC} = 3.0 V	—	1.7	—	μA
t _{d(E-A)}	Waiting time until voltage detection circuit operation starts ⁽⁴⁾		—	—	100	μs

Notes:

1. The measurement condition is V_{CC} = 1.8 V to 3.6 V and T_{opr} = –20°C to 85°C.
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.7 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{cc} rise gradient	(1)	0	—	50,000	mV/msec

Notes:

1. The measurement condition is $T_{opr} = -20^{\circ}\text{C}$ to 85°C , unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

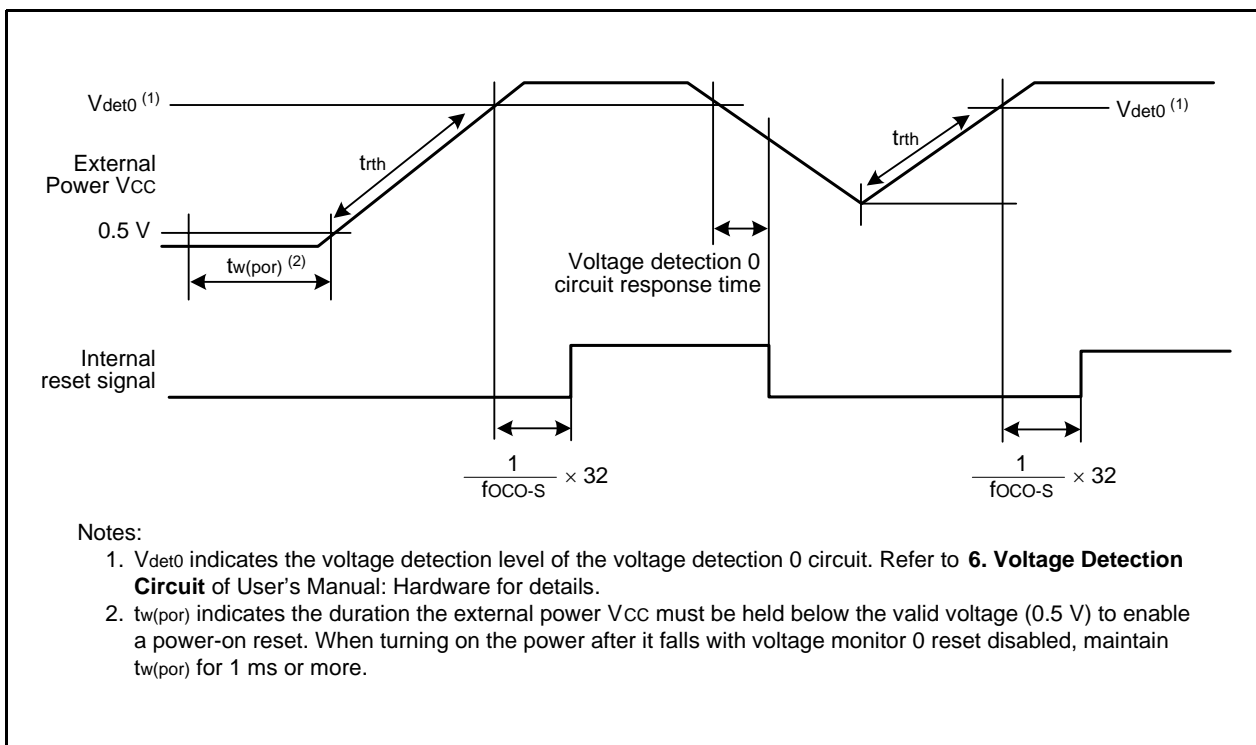


Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.8 System Clock Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-S	Low-speed on-chip oscillator frequency		100	125	150	kHz
—	Oscillation stability time		—	30	100	μs

Note:

1. $V_{CC} = 1.8\text{ V to }3.6\text{ V}$ and $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$, unless otherwise specified.

Table 5.9 Watchdog Timer Low-Speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
fOCO-WDT	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time		—	30	100	μs

Note:

1. $V_{CC} = 1.8\text{ V to }3.6\text{ V}$ and $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$, unless otherwise specified.

Table 5.10 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{d(P-R)}	Time for internal power supply stabilization during power-on (2)		—	—	2,000	μs

Notes:

1. The measurement condition is $V_{CC} = 1.8\text{ to }3.6\text{ V}$ and $T_{opr} = 25^{\circ}\text{C}$.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.

Table 5.11 Timing Requirements of Synchronous Serial Communication Unit (SSU) (1)

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
t _{SUCYC}	SSCK clock cycle time			4	—	—	t _{CYC} (2)
t _{HI}	SSCK clock "H" width			0.4	—	0.6	t _{SUCYC}
t _{LO}	SSCK clock "L" width			0.4	—	0.6	t _{SUCYC}
t _{RISE}	SSCK clock rising time	Master		—	—	1	t _{CYC} (2)
		Slave		—	—	1	μs
t _{FALL}	SSCK clock falling time	Master		—	—	1	t _{CYC} (2)
		Slave		—	—	1	μs
t _{SU}	SSO, SSI data input setup time			100	—	—	ns
t _H	SSO, SSI data input hold time			1	—	—	t _{CYC} (2)
t _{LEAD}	SCS setup time	Slave		1t _{CYC} + 50	—	—	ns
t _{LAG}	SCS hold time	Slave		1t _{CYC} + 50	—	—	ns
t _{OD}	SSO, SSI data output delay time			—	—	1.5	t _{CYC} (2)
t _{SA}	SSI slave access time		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	—	—	1.5t _{CYC} + 100	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.5t _{CYC} + 200	ns
t _{OR}	SSI slave out open time		$2.7\text{ V} \leq V_{CC} \leq 3.6\text{ V}$	—	—	1.5t _{CYC} + 100	ns
			$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$	—	—	1.5t _{CYC} + 200	ns

Notes:

1. $V_{CC} = 1.8\text{ V to }3.6\text{ V}$ and $T_{opr} = -20^{\circ}\text{C to }85^{\circ}\text{C}$, unless otherwise specified.
2. $1t_{CYC} = 1/f_1(\text{s})$

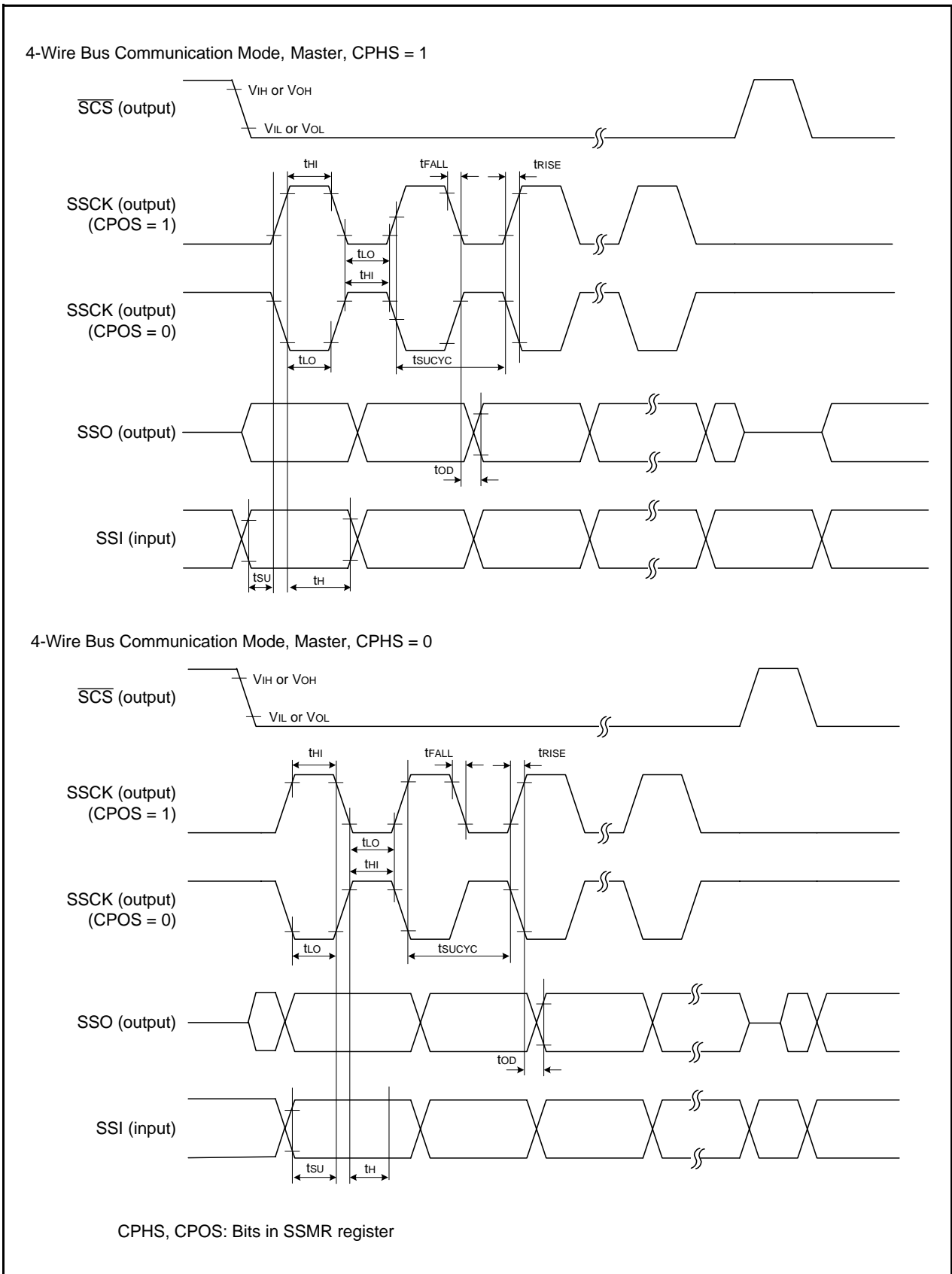


Figure 5.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

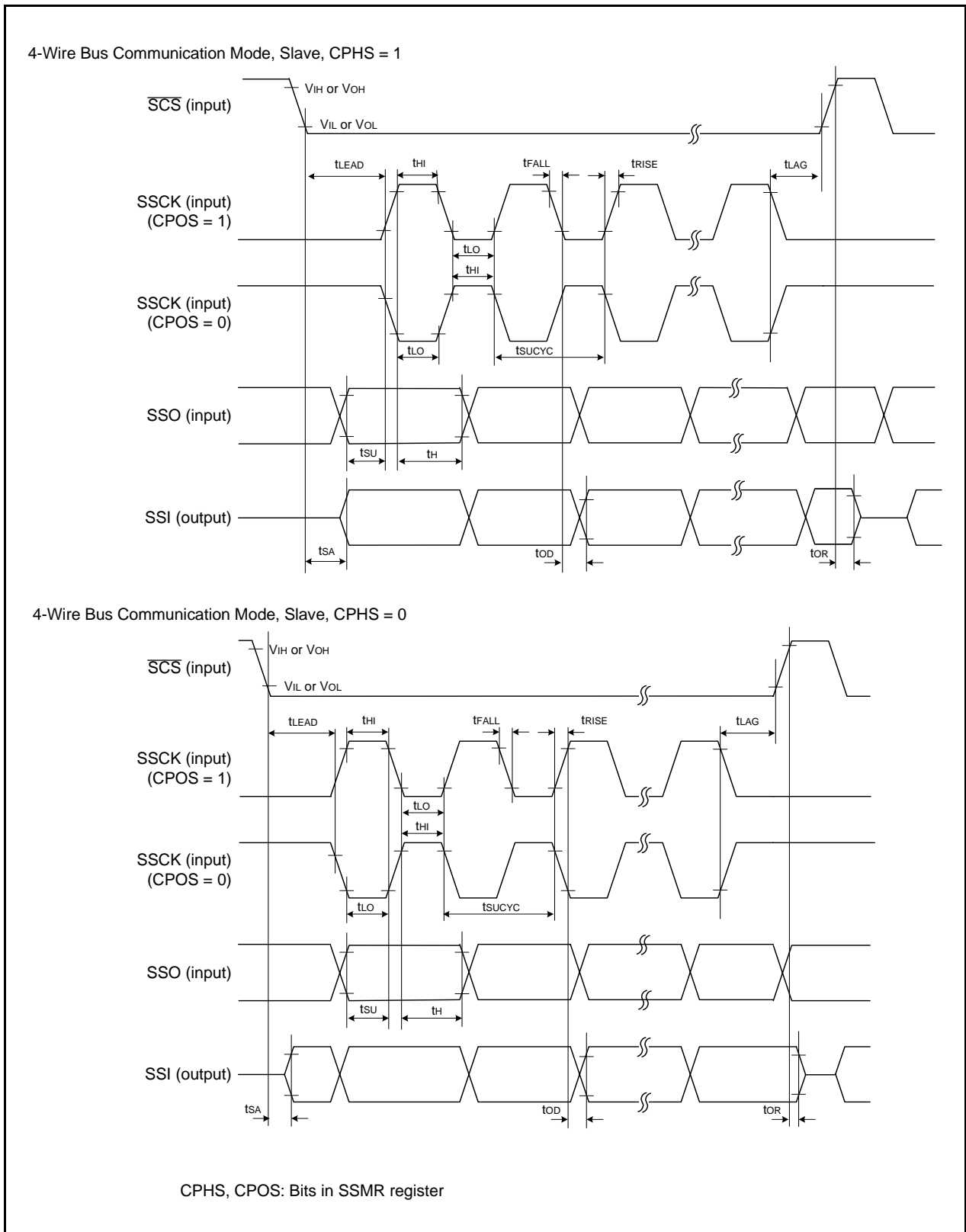


Figure 5.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

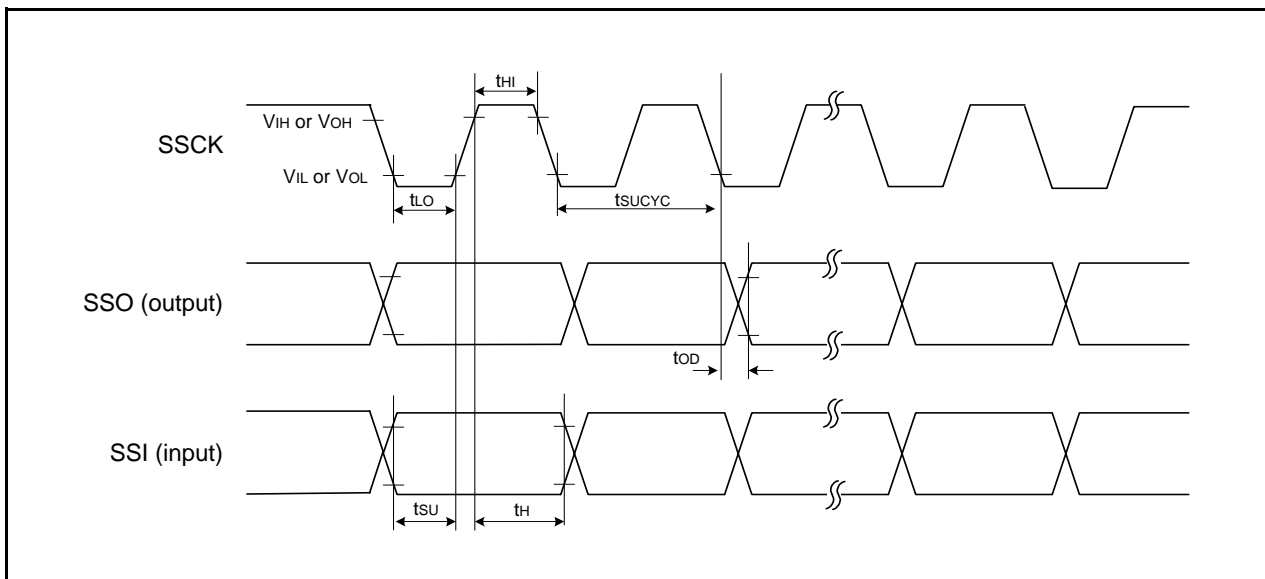


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.12 Timing Requirements of I²C bus Interface

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t _{SCL}	SCL input cycle time		12t _{cyc} + 600 ⁽²⁾	—	—	ns
t _{SCLH}	SCL input "H" width		3t _{cyc} + 300 ⁽²⁾	—	—	ns
t _{SCLL}	SCL input "L" width		5t _{cyc} + 500 ⁽²⁾	—	—	ns
t _{sf}	SCL, SDA input fall time		—	—	300	ns
t _{SP}	SCL, SDA input spike pulse rejection time		—	—	1t _{cyc} ⁽²⁾	ns
t _{BUF}	SDA input bus-free time		5t _{cyc} ⁽²⁾	—	—	ns
t _{STAH}	Start condition input hold time		3t _{cyc} ⁽²⁾	—	—	ns
t _{STAS}	Retransmit start condition input setup time		3t _{cyc} ⁽²⁾	—	—	ns
t _{STOP}	Stop condition input setup time		3t _{cyc} ⁽²⁾	—	—	ns
t _{SDAS}	Data input setup time		1t _{cyc} + 40 ⁽²⁾	—	—	ns
t _{SDAH}	Data input hold time		10	—	—	ns

Notes:

1. V_{CC} = 1.8 V to 3.6 V and T_{opr} = -20°C to 85°C, unless otherwise specified.
2. 1t_{cyc} = 1/f₁(s)

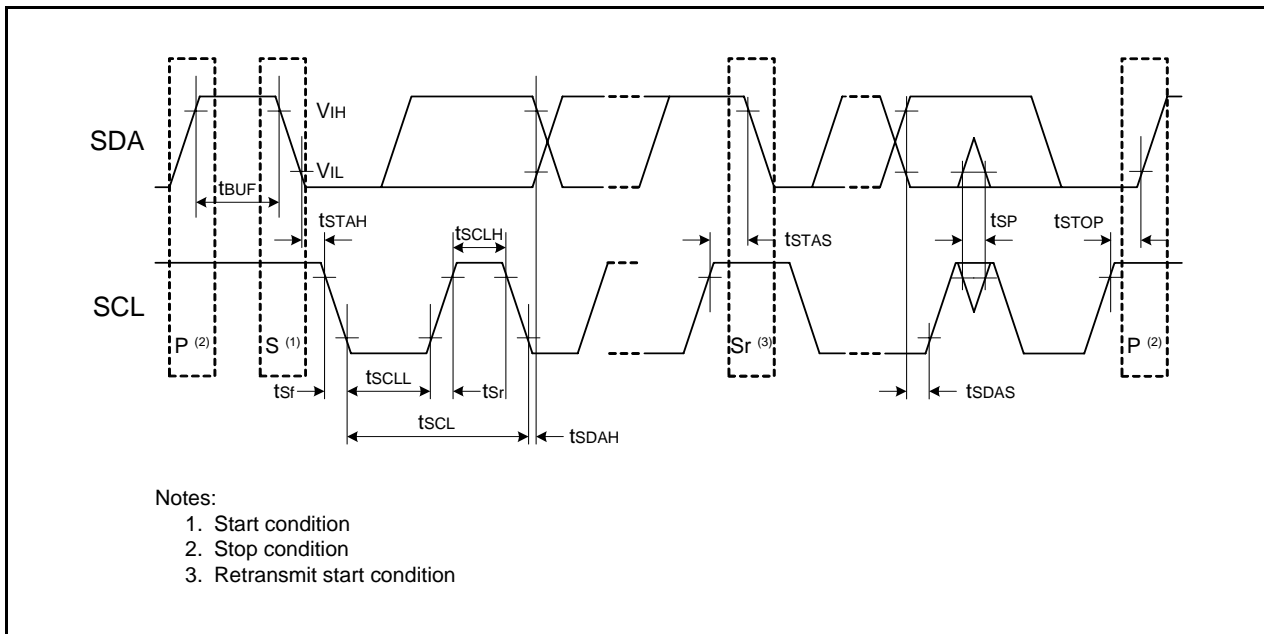
**Figure 5.7 I/O Timing of I²C bus Interface**

Table 5.13 Electrical Characteristics (1) [1.8 V ≤ Vcc ≤ 3.6 V]
(Topr = −20°C to 85°C, unless otherwise specified)

Symbol	Parameter	Condition	Standard			Unit		
			Min.	Typ.	Max.			
ICC	Power supply current Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode XIN clock oscillator on f(XIN) = 16 MHz XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = XIN	CPU clock = Divide-by-4, (f(BCLK) = 4 MHz) 1.8 V ≤ VCC ≤ 3.6 V	RF = off	—	2.5	—	mA
				RF = idle	—	4.0	—	mA
				RF = Tx	—	18	—	mA
				RF = Rx (reception standby)	—	24	—	mA
				RF = Rx (reception in progress)	—	25	—	mA
			CPU clock = Divide-by-2, (f(BCLK) = 8 MHz) 2.2 V ≤ VCC ≤ 3.6 V	RF = off	—	3.5	—	mA
				RF = idle	—	5.0	—	mA
				RF = Tx	—	19	—	mA
				RF = Rx (reception standby)	—	25	—	mA
				RF = Rx (reception in progress)	—	26	—	mA
		CPU clock = No division (f(BCLK) = 16 MHz) 2.7 V ≤ VCC ≤ 3.6 V	RF = off	—	6.0	—	mA	
			RF = idle	—	7.5	—	mA	
			RF = Tx	—	21.5	—	mA	
			RF = Rx (reception standby)	—	27.5	—	mA	
			RF = Rx (reception in progress)	—	28.5	—	mA	
		Low-speed on-chip oscillator mode XIN clock off, XCIN clock off, Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = fOCO-S, CPU clock = Divide-by-8 FMR27 = 1, VCA20 = 0 (flash memory low-current-consumption read mode)	RF = off	—	80	—	μA	
			RF = off	—	95	—	μA	
		Low-speed clock mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN CPU clock = No division	FMR27 = 1 VCA20 = 0 (flash memory low-current-consumption read mode)	RF = off	—	95	—	μA
			FMSTP = 1 VCA20 = 0 (Flash memory off, program operation on RAM)	RF = off	—	45	—	μA
		Wait mode XIN clock oscillator on: f(XIN) = 16 MHz XCIN clock oscillator on: f(XCIN) = 32 kHz Low-speed on-chip oscillator on: fOCO-S = 125 kHz System clock = XIN While a WAIT instruction is executed	RF = Rx (reception standby)	—	23	—	mA	
Wait mode XIN clock off XCIN clock oscillator on f(XCIN) = 32 kHz Low-speed on-chip oscillator off System clock = XCIN While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	6.0	—	μA		
	Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal power consumption enabled)	RF = off	—	4.5	—	μA		
Wait mode XIN clock off XCIN clock oscillator on Low-speed on-chip oscillator on fOCO-S = 125 kHz System clock = fOCO-S While a WAIT instruction is executed	Peripheral function clock on VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	13.0	—	μA		
	Peripheral function clock off VCA26 = VCA25 = 0 VCA20 = 1 (voltage detection circuit stopped, internal low power consumption enabled)	RF = off	—	7.5	—	μA		
Stop mode (Topr = 25°C) XIN clock off, XCIN clock off, Low-speed on-chip oscillator off, VCA26 = VCA25 = 0 (voltage detection circuit stopped)	RF = off	—	2.0	—	μA			

Table 5.14 Electrical Characteristics (2) [2.7 V ≤ V_{CC} ≤ 3.6 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I _{OH} = -5 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I _{OL} = 5 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, KI4, KI6, KI7, TRAIO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0, SSI, SCL, SDA, SSO	V _{CC} = 3.0 V		0.1	0.4	—	V
		RESET	V _{CC} = 3.0 V		0.1	0.5	—	V
I _{IH}	Input "H" current		V _I = 3 V, V _{CC} = 3.0 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 3.0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 3.0 V		42	84	168	kΩ
R _{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	3.6	V

Note:

- 2.7 V ≤ V_{CC} ≤ 3.6 V, T_{opr} = -20°C to 85°C, and f(XIN) = 16 MHz, unless otherwise specified.

Timing requirements (VCC = 3 V, Topr = -20°C to 85°C, unless otherwise specified)

Table 5.15 TRAI0 Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc(TRAIO)	TRAIO input cycle time	300	—	ns
tWH(TRAIO)	TRAIO input "H" width	120	—	ns
tWL(TRAIO)	TRAIO input "L" width	120	—	ns

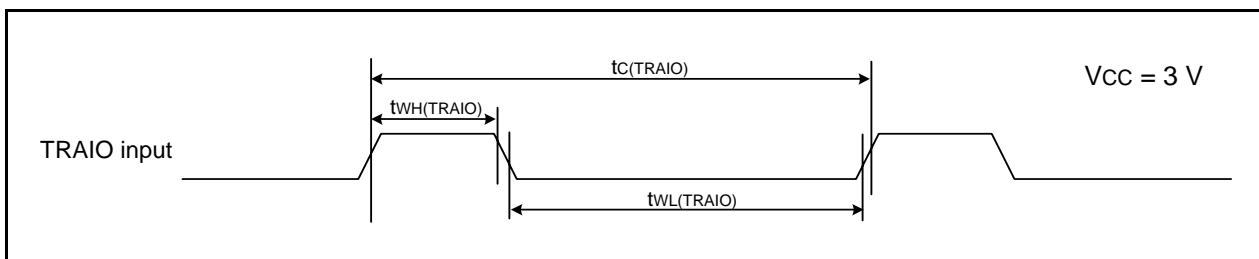


Figure 5.8 TRAI0 Input Timing Diagram when Vcc = 3 V

Table 5.16 Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
tc(CLK)	CLK0 input cycle time	When an external clock is selected	300	—	ns
tW(CKH)	CLK0 input "H" width		150	—	ns
tW(CKL)	CLK0 Input "L" width		150	—	ns
td(C-Q)	TXD0 output delay time		—	120	ns
th(C-Q)	TXD0 hold time	When an internal clock is selected	0	—	ns
tsu(D-C)	RXD0 input setup time		30	—	ns
th(C-D)	RXD0 input hold time		90	—	ns
th(C-Q)	TXD0 output delay time		—	30	ns
tsu(D-C)	RXD0 input setup time		120	—	ns
th(C-D)	RXD0 input hold time		90	—	ns

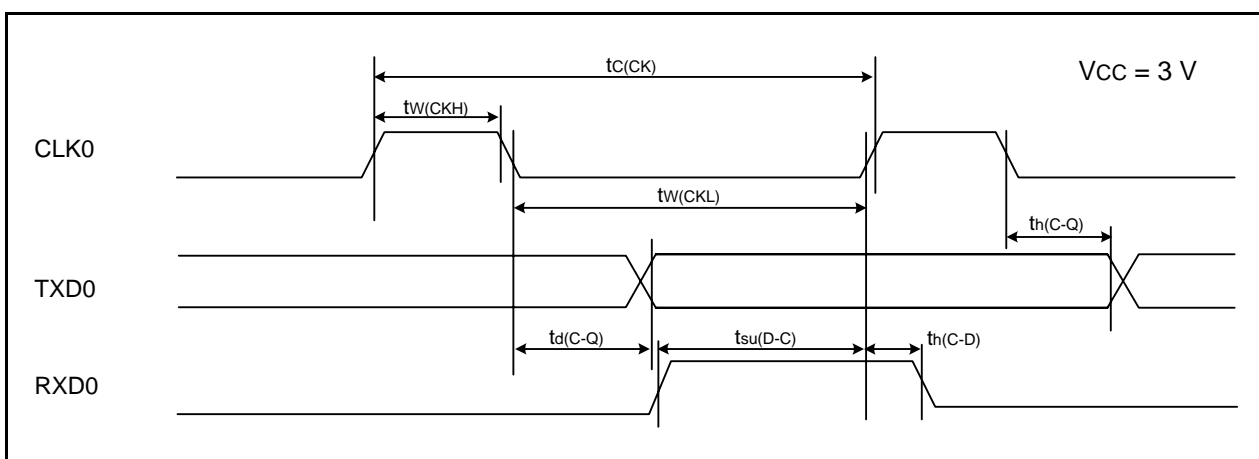


Figure 5.9 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.17 External Interrupt $\overline{\text{INT}}_i$ ($i = 0, 1, 3$) Input, Key Input Interrupt $\overline{\text{K}}_i$ ($i = 0$ to 7)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(\text{INH})}$	$\overline{\text{INT}}_i$ input "H" width, $\overline{\text{K}}_i$ input "H" width	380 ⁽¹⁾	—	ns
$t_{W(\text{INL})}$	$\overline{\text{INT}}_i$ input "L" width, $\overline{\text{K}}_i$ input "L" width	380 ⁽²⁾	—	ns

Notes:

1. When selecting the digital filter by the $\overline{\text{INT}}_i$ input filter select bit, use an $\overline{\text{INT}}_i$ input HIGH width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{\text{INT}}_i$ input filter select bit, use an $\overline{\text{INT}}_i$ input LOW width of either (1/digital filter clock frequency \times 3) or the minimum value of standard, whichever is greater.

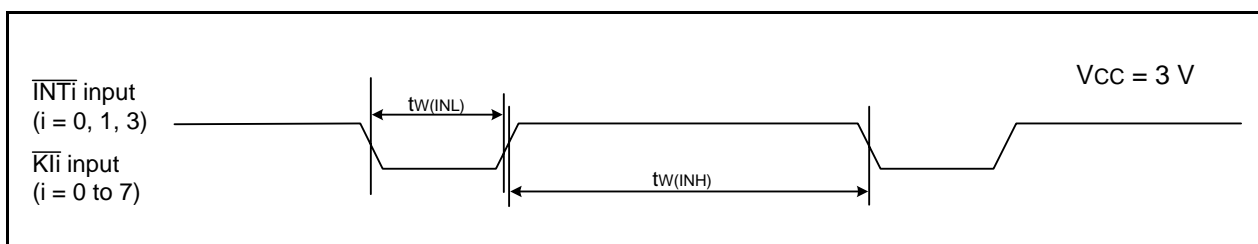
**Figure 5.10 Input Timing Diagram for External Interrupt $\overline{\text{INT}}_i$ and Key Input Interrupt $\overline{\text{K}}_i$ when $V_{CC} = 3\text{ V}$**

Table 5.18 Electrical Characteristics (3) [$1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$]

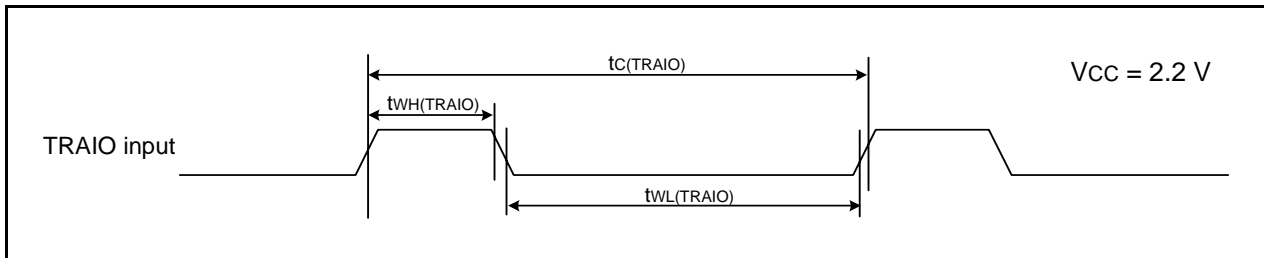
Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I _{OH} = -2 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity Low	I _{OH} = -1 mA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	P0_4, P1, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_5	Drive capacity High	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity Low	I _{OL} = 1 mA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT3, KI0, KI1, KI2, KI3, KI4, KI6, KI7, TRAI0, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRCTRG, TRCCLK, RXD0, CLK0, SSI, SCL, SDA, SSO	V _{CC} = 2.2 V		0.05	0.20	—	V
		RESET	V _{CC} = 2.2 V		0.05	0.20	—	V
I _{IH}	Input "H" current		V _I = 2.2 V, V _{CC} = 2.2 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V, V _{CC} = 2.2 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V, V _{CC} = 2.2 V		70	140	300	kΩ
R _{IXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R _{IXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V _{RAM}	RAM hold voltage		During stop mode		1.8	—	3.6	V

Note:

1. $1.8\text{ V} \leq V_{CC} < 2.7\text{ V}$, T_{opr} = -20°C to 85°C, and f(XIN) = 16 MHz, unless otherwise specified.

Timing requirements ($V_{CC} = 2.2\text{ V}$, $T_{opr} = -20^{\circ}\text{C}$ to 85°C , unless otherwise specified)**Table 5.19** TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	500	—	ns
$t_{WH(TRAIO)}$	TRAIO input "H" width	200	—	ns
$t_{WL(TRAIO)}$	TRAIO input "L" width	200	—	ns

**Figure 5.11** TRAIO Input Timing Diagram when $V_{CC} = 2.2\text{ V}$ **Table 5.20** Serial Interface

Symbol	Parameter		Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLK0 input cycle time	When an external clock is selected	800	—	ns
$t_{W(CKH)}$	CLK0 input "H" width		400	—	ns
$t_{W(CKL)}$	CLK0 input "L" width		400	—	ns
$t_{d(C-Q)}$	TXD0 output delay time		—	200	ns
$t_{h(C-Q)}$	TXD0 hold time	When an internal clock is selected	0	—	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns
$t_{h(C-Q)}$	TXD0 output delay time		—	200	ns
$t_{su(D-C)}$	RXD0 input setup time		150	—	ns
$t_{h(C-D)}$	RXD0 input hold time		90	—	ns

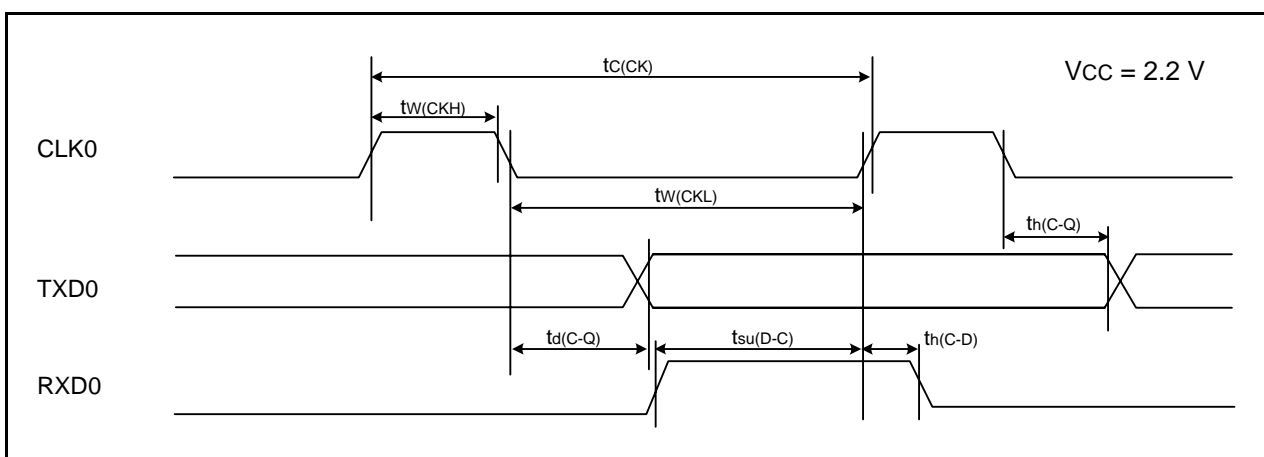
**Figure 5.12** Serial Interface Timing Diagram when $V_{CC} = 2.2\text{ V}$

Table 5.21 External Interrupt \overline{INTi} (i = 0, 1, 3) Input, Key Input Interrupt \overline{Kli} (i = 0 to 7)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	\overline{INTi} input "H" width, \overline{Kli} input "H" width	1000 (1)	—	ns
$t_{W(INL)}$	\overline{INTi} input "L" width, \overline{Kli} input "L" width	1000 (2)	—	ns

Notes:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

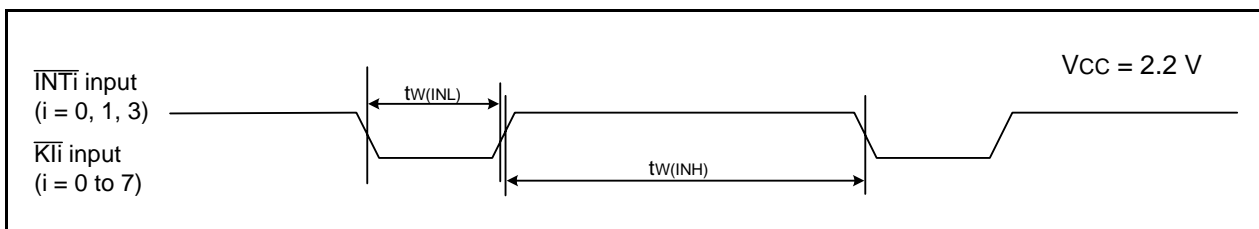


Figure 5.13 Input Timing Diagram for External Interrupt \overline{INTi} and Key Input Interrupt \overline{Kli} when $V_{CC} = 2.2 V$

Table 5.22 Transceiver Transmission Characteristics
(VCC = VCCRF = 3.3 V, Topr = 25°C, unless otherwise specified)

Parameter		Condition	Standard			IEEE802.15.4 standard	Unit
			Min.	Typ.	Max.		
Internal voltage			—	1.45	—	—	V
Nominal output power			-3	0	3	-3 or more	dBm
Transmit bit rate			—	250	—	250	kbps
Transmit chip rate			—	2000	—	2000	kchips/s
Programmable output power range		32 steps	—	32	—	32 steps	dB
Harmonics	2nd harmonics	External notch filter	—	—	-47.2	-41.2 or less	dBm
	3rd harmonics		—	—	-47.2	—	
Spurious emission	30 – 88 MHz	Maximum output power, Renesas evaluation board	—	—	-55.2	FCC	dBm
	88 – 216 MHz		—	—	-51.7	FCC	
	216 – 960 MHz		—	—	-49.2	FCC	
	960 – 1000 MHz		—	—	-41.2	FCC	
	1 – 12.75 GHz		—	—	-41.2	FCC (1)	
	1.8 – 1.9 GHz		—	—	-47	ETSI	
Error vector magnitude EVM		1000 chips	—	—	35	35 or less	%
Power spectral density	Absolute limit	f-fc > 3.5 MHz	—	—	-30	-30 or less	dBm
	Relative limit	f-fc > 3.5 MHz	—	—	-20	-20 or less	dB
Frequency tolerance		Including crystal ±20 ppm	-40	—	40	Within ±40	ppm

Note:

1. Notes on FCC certification testing

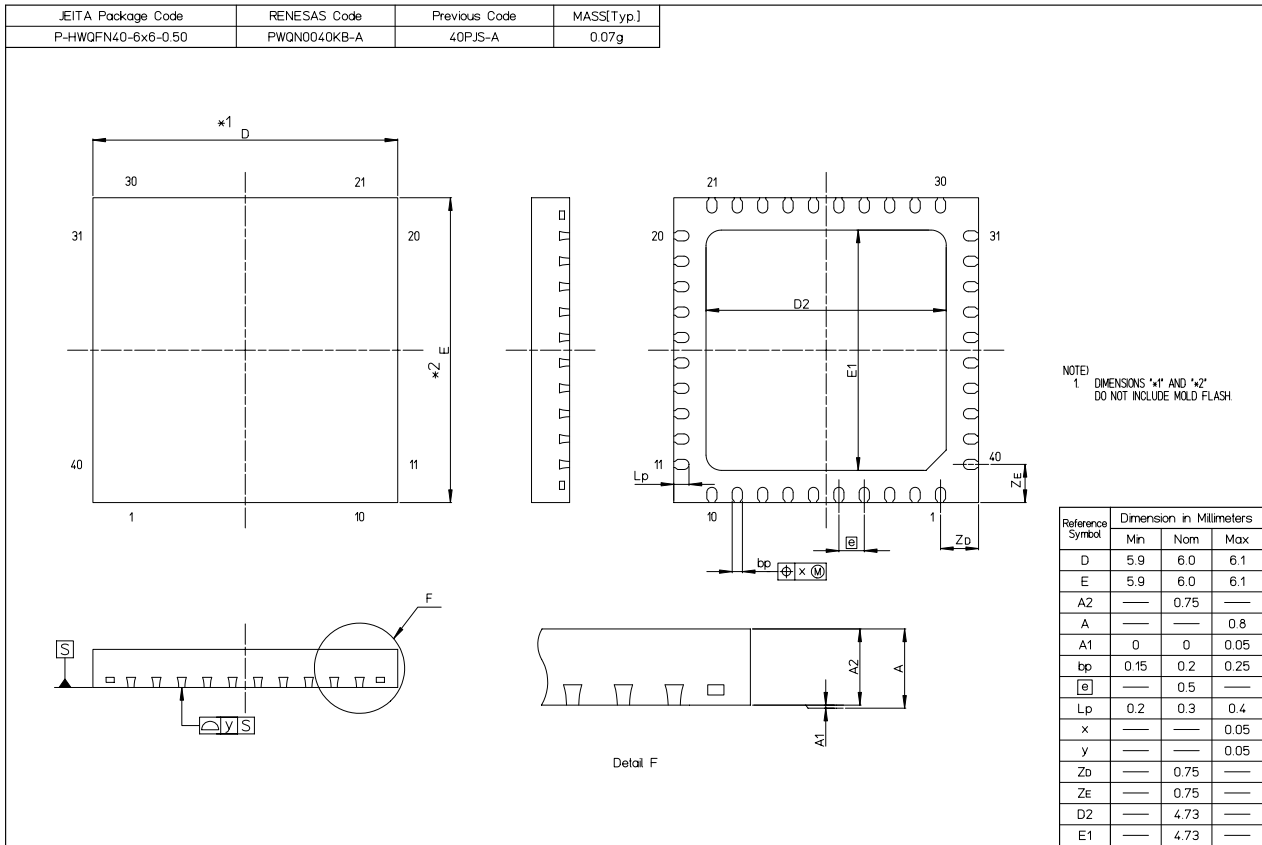
When using 26 CH (2480 MHz), adjust the transmit power to meet the FCC requirements and standards at 2483.5 MHz.

Table 5.23 Transceiver Reception Characteristics
(VCC = VCCRF = 3.3 V, Topr = 25°C, unless otherwise specified)

Parameter		Condition	Standard			IEEE802.15.4 standard	Unit
			Min.	Typ.	Max.		
Internal voltage			—	1.45	—	—	V
RF input frequency			2405	—	2480	Min. 2405/ Max. 2480	MHz
Receiver sensitivity		PER = 1% PSDU Length = 20 octets Interframe spacing 12 symbols (IEEE802.15.4 minimum spacing)	—	-95	-85	-85 or less	dBm
Maximum input level		PER = 1%	0	—	—	-20 or more	dBm
Adjacent channel rejection	+5 MHz	PER = 1%	0	—	—	0 or more	dB
	-5 MHz	Prf = -82 dBm	0	—	—		
Alternate channel rejection	+10 MHz	PER = 1%	30	—	—	30 or more	dB
	-10 MHz	Prf = -82 dBm	30	—	—		
Rejection	> +15 MHz	PER = 1%	30	—	—	—	dB
	< -15 MHz	Prf = -82 dBm	30	—	—		
Spurious emission	30 – 1000 MHz	Renesas evaluation board	—	—	-57	ETSI EN300/328	dBm
	1 – 12.75 GHz		—	—	-47		
Symbol error tolerance			-80	—	80	±80 or less	ppm
RSSI range		Prf (min) = -75 dBm	40	75	—	40 or more	dB
RSSI accuracy		Prf = -75 to -35 dBm	-6	—	6	Within ±6	dB

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.



REVISION HISTORY	R8C/3MQ Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Nov 19, 2010	—	First Edition issued
1.00	Aug 11, 2011	All pages	“Preliminary”, “Under development” deleted
		4	Table 1.2 revised, Note 1 added
		5	Table 1.3 “(D): Under development”, (P): Under planning” deleted
		6	Figure 1.2 revised
		7	Figure 1.3 revised
		9, 10	Table 1.5, Table 1.6 revised
		12	2.4 revised
		14	3.1 revised
		16, 17	Table 4.2, Table 4.3 revised
		19	Table 4.5 Note 2 added
		20	Table 4.6 revised
		24, 25	Table 4.10, Table 4.11 revised
		32	Table 5.6 revised
		39	Table 5.13 revised
		46	Table 5.22, Table 5.23 revised, Table 5.22 Note 1 added

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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